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UNITED STATES DEPARTMENT OF ENERGY
UNIVERSITY CENTER OF EXCELLENCE
FOR PHOTOVOLTAIC RESEARCH AND EDUCATION

February 7, 2006

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RE: NREL Subcontract # ADJ-1-30630-12

Dear Ken,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of December 9, 2005 to January 9, 2006 under the subject subcontract. The report highlights progress and results obtained under Task 3 (Si-based Solar Cells) and Task 4 (In-Line Diagnostics).

TASK 3: SI-BASED SOLAR CELLS

Aluminum Induced Crystallization

In the monthly report for October 2005, a design of experiment (DOE) approach was described to continue the study of aluminum induced crystallization (AIC) of Al-Si bilayers. A matrix of samples was created to investigate key variables that had been identified by previous AIC studies at IEC. We are looking for the effect of different structures (normal and reverse), different annealing temperature (above and below eutectic), and annealing time on AIC. The experiments were designed to evaluate the effects of 3 factors on AIC as shown in Table I.

Table I. High and low values of parameters for DOE study of AIC

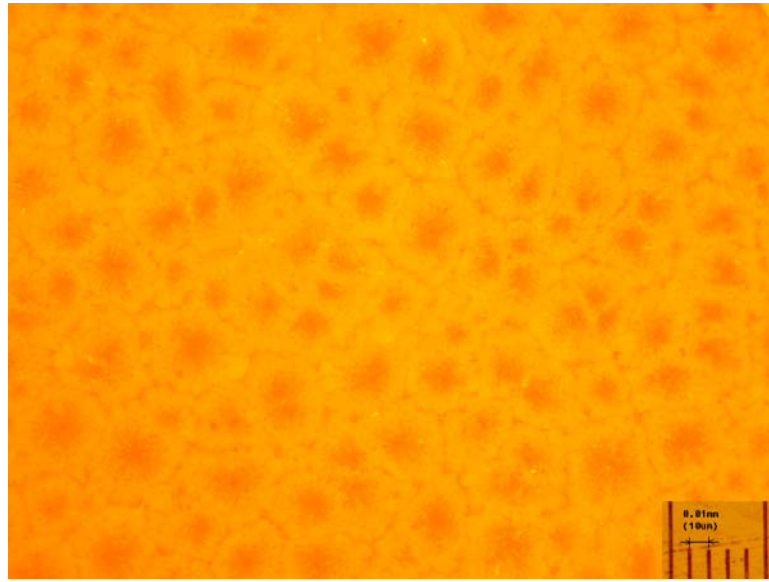
Name	Low value	High value
Temperature:	450°C (<Eu.T)	600°C (>Eu.T)
Time:	1hr	6 hr
Structure:	Normal (500nm a-Si/ 400nm Al /substrate 1737)	Reverse (400nmAl/ 500nm a-Si / substrate 1737)

The DOE approach indicated a matrix of 8 samples as described in the October report. Si and Al layers are deposited by e-beam. In both normal and reverse structure, the a-Si layer is 500nm, and the Al layer is 400nm. Since the e-beam system can hold 9 substrates per run, additional substrates were added to the matrix, including mono and multi c-Si wafers, and ceramic.

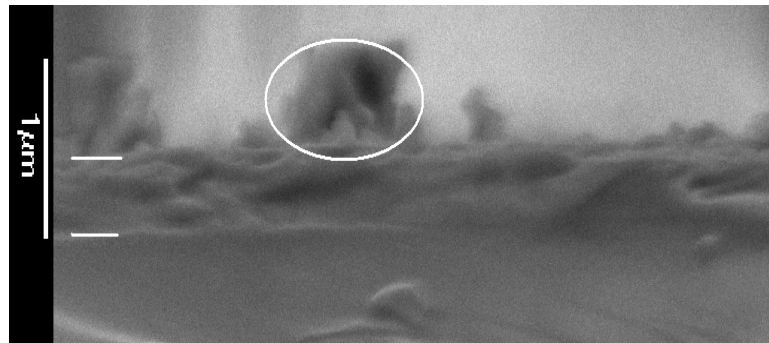
All samples have been annealed and sequentially etched, Al etching in H_3PO_4 and a-Si or nc-Si etching in XeF_2 , to reveal the underlying c-Si layer. Measurements performed either before, during or after etching included optical microscopy (OM), XRD, AFM, Raman and SEM. Here we report some preliminary results.

1. From the DOE samples on 1737 glass, we obtained the some new results for etched samples comparing to the one before etching:

- (a) **450°C, 6 hr, normal structure.** We obtains “grains” about $\sim 30\mu m$ size based on OM reflection measurement shown in Figure 1a taken from the glass side. The SEM image and the cross section for etched samples show these “grains” form a continuous silicon layer with extra silicon peaks standing out of the surface (see Figure 1b). Under SEM, the “grain” seems to be single-crystal, but this should be confirmed by TEM measurement.



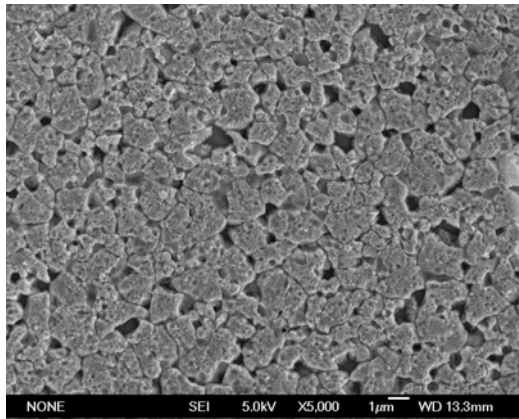
(1a)



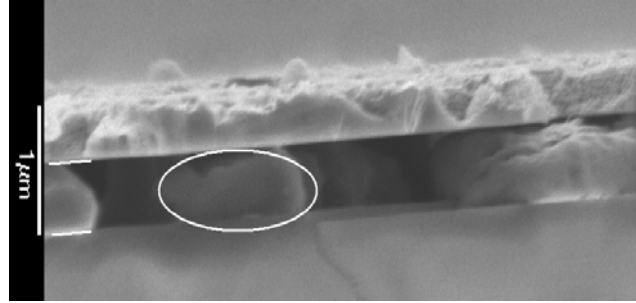
(1b)

Figure 1. Samples on 1737 glass annealed @ 450°C for 6 hr, normal structure. (a) top, OM reflection image taken from glass side. Each interval in the bar grid corresponds to 10um, most of the grains are more than 30 μm. (b) bottom, SEM cross section, where the white lines show Si film ~0.5 μm, and the circle highlight extra Si peaks on surface of continuous Si grains.

- (b) 450°C, 6 hr, reverse structure.** We have already shown the nucleation density is much larger than the normal structure, and the “grain” of silicon is smaller. This is clearer under SEM image (Figure 2a), which shows the “grain” size is about 1-2μm. Also, the cross section image (Figure 2b) proves the silicon layer is on the top, with bottom Al layer etched away, and some additional silicon underneath supporting the continuous layer on top.



(2a)



(2b)

Figure 2. 1737 samples annealed @ 450°C for 6 hr, reverse structure.

(a) SEM image. (b) Cross section. The white line is guidance for view, and the circle highlight extra Si left in bottom.

- (c) **600°C, 6 hr, normal structure.** This treatment resulted in a large degree of non-uniformity of the thickness and composition. The latter is well shown in the SEM image and corresponding elemental mapping. Figure (3a) is SEM image, (3b) and (3c) are corresponding elemental mapping of silicon and aluminum. Figure 3b is the Si mapping of the SEM image with white indicating high Si and dark indicating low Si. Figure (3c) is the corresponding Al map. Some Al remains after etching, indicating it is intermixed with Si as in a Si-Al alloy.



(3a)

(3b)

(3c)

Figure 3. 1737 samples annealed @ 600°C for 6 hr, normal structure.

(a) SEM image. (b) and (c) are corresponding elemental mapping, with (b) silicon and (c) aluminum.

- (d) **600°C, 6 hr, reverse structure.** This condition gives an interesting result. We got a continuous Si layer on the top, but we cannot tell the “grain size” from SEM (Figure 4a). TEM should be done to get more detailed information, but Raman (Figure 4b) confirms the top layer is crystallized Si.

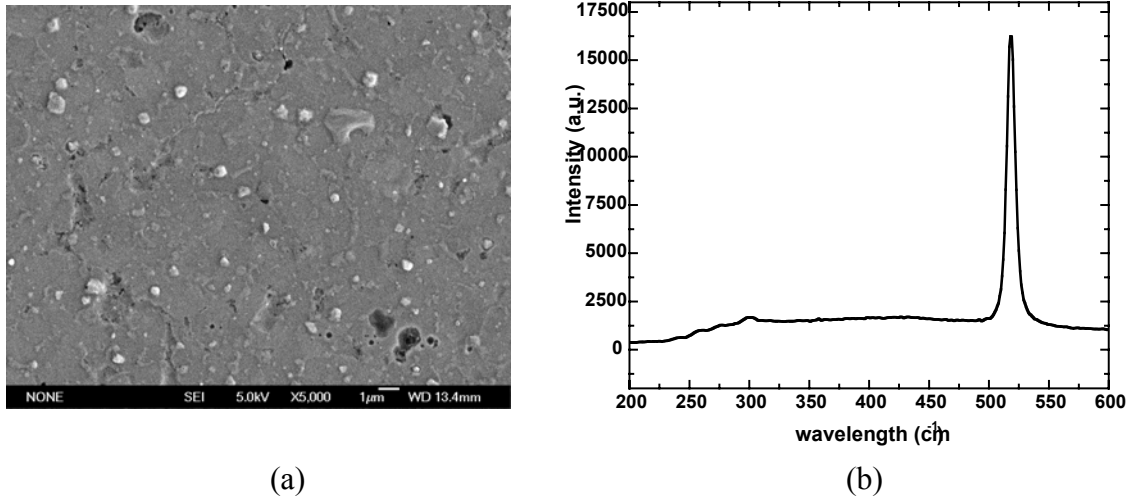


Figure 4. (a) SEM image and (b) Raman spectrum for 1737 samples annealed @ 600°C for 6 hr, reverse structure.

The following are the results on non-glass substrates:

- (a) **Samples on c-Si wafer, @ 450°C, normal structure.** The annealed sample has the same XRD pattern as the substrate suggesting either epitaxial growth or no crystallization occurred. Raman measurement proves there was no crystallization. This is unexpected, and suggests results may depend on the orientation of substrates or surface cleaning. Further work is needed to understand epitaxial growth in the AIC process.
- (b) **Samples on c-Si wafer, @ 600°C, normal structure.** The XRD gives the same pattern as substrate, but Raman confirms the top layer is crystallized Si. Thus, the crystallized layer has the same orientation as substrate. Also, Figure 5 shows that there is an unusual signal in Raman spectrum at about 440cm⁻¹. We believe that's due to the little Al left in Si, since the sample was annealed at 600°C (> eutectic T). Further, the SEM cross section image shows the Si wafer surface is no longer smooth and that the Si film is non-continuous, suggesting the Al layer reacted with the bottom c-Si wafer.

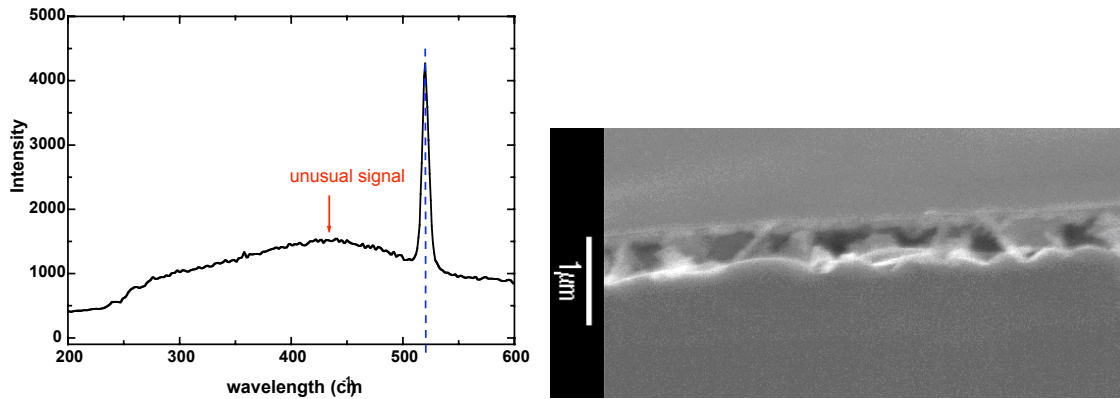


Figure 5. Raman spectrum (left) and cross section image (right) for sample on c-Si wafer, 600°C, normal structure, showing roughened Si wafer surface.

- (c) **On ceramic, @ 450°C, normal structure.** We are getting a continuous Si layer, similar with the one on glass 1737, but due to the roughness of ceramic, grain size hasn't been determined yet.
- (d) **On ceramic, @ 600°C.** For **normal structure**, we got uniform and continuous silicon layer. For **reverse structure**, the crystallized silicon layer is not quite continuous. For both cases, due to the roughness of ceramic, grain size hasn't been determined yet.

As a summary, these results show that the following conditions may lead to promising conditions for growth of continuous, large grain silicon layer (such as for seed layer for subsequent growth of thicker Si film):

Table II. Summary of AIC above and below Eutectic T.

Condition	Resulting Si-layer
(a) glass1737, < Eu.T., normal	continuous, grain: $\sim 30\mu\text{m}$
(b) glass1737, > Eu.T., reverse	continuous, grain: can't tell in OM & SEM
(c) wafer, > Eu.T., normal	continuous network
(d) ceramic, > Eu.T., normal	continuous, grain: not sure due to roughness

Solid phase crystallization (SPC)

There are several groups using SPC of a-Si p-n junctions on glass at $\sim 600^\circ\text{C}$ for 24-48 hr to make c-Si p-n junction solar cells. Recently, the group at UNSW reported devices with

$V_{oc}=0.45$ V made by SPC at 600°C for 48 hr followed 1-10 min rapid thermal processing (RTP) at 900°C.¹ The 1.8 μm a-Si was deposited by e-beam, therefore, had no H. A post-RTP plasma hydrogenation was crucial to increase V_{oc} and reduce shunting. The substrate is borosilicate glass without any TCO.

Previously, we explored SPC and RTA of plasma, hot wire, and e-beam deposited a-Si films and found negligible crystallization of the e-beam films for either SPC or RTP. This suggested that H is needed for crystallization in contrast to the UNSW results with e-beam a-Si. Therefore, we designed a set of experiments to identify any role of H in the film. We did SPC for 24 and 48 hr using 1.5 μm HWCVD a-Si films on 7059 glass. One group of substrates had no prior dehydrogenation. The other group had 4 hr at 400°C and 4 hr at 500°C, prior to SPC at 600°C. Following SPC, XRD and AFM was measured to determine grain size. Results are in Table III. The grain size is 70-100 nm, which is about a factor of 2 larger than was found for RTP on comparable films. Figure 6 shows the AFM image; small grains, ~ 0.1 μm consistent with the XRD in Table III, forming dense aggregates leading to larger apparent features. While larger than as-deposited nanocrystalline Si films, the grain size is at least a factor of 20 smaller than the grains reported by UNSW, Kaneka, and others using SPC. It is not clear that dehydrogenation has a significant effect. Samples will be given an RTP at 800-900°C to determine if that process results in further grain enhancement.

Table III. Grain size from XRD for a-Si films with 24 and 48 hr SPC at 600°C.

Piece	Dehydrogenation	SPC	Grain Size (nm)
HW272-31a	None	24 hr	75
HW272-31c	None	48 hr	69
HW272-12a, b	400/500°C	24 hr	95
HW272-21a, b	400/500°C	48 hr	71
HW269-12	400/500°C	None	None

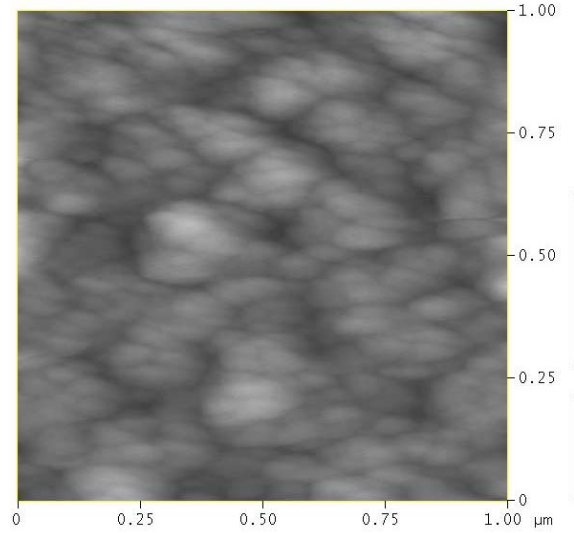


Figure 6. AFM image of HW272-12 after SPC.

Table IV lists device structures that were deposited by HWCVD for further SPC and RTP study. HW281 (n+/i) and HW283 (p+/i) are partially completed devices while HW282 (n+/i/p+) and HW284 (p+/i/n+) are completed devices. Conditions for the doped layers were the same except for the dopant gas. After SPC and/or RTP, samples will be given plasma hydrogenation and 281 and 283 will receive top doped layers. There were 4 types of substrates: (1)7059 glass (2) ZnO on 1737 (3) ZnO on 7059 (4) SnO₂ – Tec 15, in each run. Raman measurements verified that there is no nc-Si in these devices.

Table IV. Device structures deposited by HWCVD.

Run #	Structure
HW281	Substrate / a-Si:H.n+ (20nm) / a-Si:H.i (1.5 μm)
HW282	Substrate / a-Si:H.n+ (20nm) / a-Si:H.i (1.5 μm) / a-Si:H.p+ (20nm)
HW283	Substrate / a-Si:H.p+ (20nm) / a-Si:H.i (1.5 μm)
HW284	Substrate / a-Si:H.p+ (20nm) / a-Si:H.i (1.5 μm) / a-Si:H.n+ (20nm)

TASK 4: IN-LINE PROCESS DIAGNOSTICS

Significant effort has been made to develop the contact wetting angle as a diagnostic to monitor the evolution of surface properties as reported in previous monthly reports. Our first paper on this subject has been accepted for publication in Progress in Photovoltaics. The title is “Contact Wetting Angle as a Characterization Technique for Processing CdS/CdTe Solar Cells,” M.S. Angelo, B.E. McCandless, R.W. Birkmire, S.A. Rykov, and J.G. Chen.

Best regards,

A handwritten signature in black ink, appearing to read 'Robert Birkmire', with a stylized, cursive script.

Robert W. Birkmire
Director

RWB/bj

Cc: Paula Newton, IEC
Steven Hegedus, IEC
Ujjwal Das, IEC
Gerri Hobbs, OVPR, UD
Carolyn Lopez, NREL

References

¹ M.L. Terry, A. Straub, D. Inns, D. Song, and A.G. Aberle, Appl. Phys. Lett. **86**, 172108 (2005).